THAT WHICH IS CLAIMED IS:

1. A memory device comprising a standard flash memory core, a micro-controller for managing standard flash memory functions, testing of the device at wafer level and as finished product, redundancy analysis, programming of re-routing cams and validation of the device, a test mode command interface (TUI) for coupling with an external test equipment, a circuit block (REPAIR-DATA_GEN) including a register (REDUNDANCY_REGISTER) on which a redundancy vector to be programmed in said re-routing cams and the selected paths for programming information are stored during execution of a cam programming algorithm, characterized in that it comprises an in-built hardware structure for performing predefined routines of testing, redundancy analysis, programming of re-routing cams and validation of the device internally without exchanging data with said external test equipment, comprising the following functional circuit blocks:

a first cache memory (LOCAL ADDRESS CACHE) for storing up to a maximum number N of column addresses in which failed cells are detected, equal to the number of column redundancy resources available for each sector of the standard memory array;

an address counter (DEVICE ADDRESS COUNTER);

a circuit (EXPECTED DATA GENERATION) for generating the expected datum from reading a certain memory location pre-programmed with said expected datum;

a circuit (DATA COMPARISON) for comparing said generated expected with the datum read from said memory location;

an number N of registers (LOCAL DATA CACHE) equal to the number of column redundancy resources available for each sector of the standard memory array, each register having a number M of bits coinciding with the read parallelism of the standard memory array, and in which said comparison circuit (DATA COMPARISON) writes information relatives to the bits on which a failure has occurred;

a counter of modulus M (BIT POSITION COUNTER) for bit by bit scanning said N registers (LOCAL DATA CACHE);

an up/down counter (RESOURCE COUNTER) for pointing to one of the register of said N registers (LOCAL DATA CACHE), to one of the registers of said first cache memory (LOCAL ADDRESS CACHE) and to a location of a second cache memory (GLOBAL CACHE) and including a latch for preserving a pointer value;

said second cache memory (GLOBAL CACHE) for storing in a compressed form information relative to failed array cells detected in a certain sector, accessed, in reading and in writing, through a first data bus (GLB_CACHE_DATA) and controlled through a second bus (EXT_RD_WR_INTERFACE) coming from said test mode command interface (TUI) or through a third bus (GLB_CACHE_CTRL_BUS) coming from said micro-controller (MICRO) ;

a cache address generator (CACHE ADDRESS GENERATOR) for generating the current address of the second cache memory (GLOBAL CACHE) from the address current in said address counter (DEVICE ADDRESS COUNTER) and the content of said up/down counter (RESOURCE COUNTER);

a plurality of bus drivers, driven by control signals (WRITE_FAIL_INFO, WRITE_RESOURCE_INFO,

WRITE_GLB) managed by said micro-controller (MICRO), for accessing said first data bus (GLB_CACHE_DATA) and thence said second cache memory (GLOBAL_CACHE) for writing therein the following information:

a) the content (RESOURCE_INFO) of said up/down counter (RESOURCE_COUNTER);

b) the information of the position of the detected failed bits in a compressed form (POSITION_INFO) derived from scanning said N registers (LOCAL DATA CACHE) through said counter of modulus M (BIT POSITION COUNTER);

c) the column address (ADDRESS_INFO) of columns with detected failed cells;

d) information written in said second cache memory (GLOBAL_CACHE) through said test mode command interface (TUI) for executing specific test routines.

2. The memory device according to claim 1, wherein the address (SECTOR_ADD) current in said address counter (DEVICE ADDRESS COUNTER) is fed to a first pointer generator (SECTOR POINTER GENERATOR) and the content (RESOURCE_ADD) of said up/down counter (RESOURCE COUNTER) is fed to a second pointer generator (RESOURCE OFFSET GENERATOR), and the data output by said first and second pointer generators are combined by a binary adder coupled to a first input (A) of a multiplexer (MUX), to a second input (B) of which an address of a cache memory location is applicable from outside through said interface (TUI), for the selection of the access mode driven by an external command signal (USE_EXT_ADDRESS / USE_MSEQ_ADDRESS) through said interface (TUI).

3. The memory device according to claim 1, wherein said second cache memory (GLOBAL_CACHE) is addressable also through said program counter (PROGRAM_COUNTER) used for addressing the read only memory of the micro-controller, the pointer datum (MICRO ADDRESS) being fed to a third input (C) of said access mode multiplexer (MUX).